ASYMMETRY CORRECTION FOR MAGNETO-RESISTIVE HEADS

ABSTRACT OF THE DISCLOSURE

An asymmetry-reducing circuit adapted to process an input signal having positive and negative pulses of different amplitudes and generate a corresponding balanced signal having positive and negative pulses of substantially uniform amplitudes. The asymmetry-reducing circuit balances the input signal by providing signal contributions corresponding to the second and third orders of the input signal. In a representative embodiment, the asymmetry-reducing circuit includes a differential amplifier and a plurality of arrayed MOS transistors connected to its inputs and outputs such that source-to-drain conductance of the transistors provides input and feedback resistances to the amplifier. A switch set selectively couples the fingers (gates) of the transistors to the input signal to modulate the source-to-drain conductance with said signal such that the input and feedback resistances change in a complementary manner. Advantageously, circuits of the invention can correct signal asymmetry within a relatively wide asymmetry range.